REMARKS

This is a response to the Office Action mailed January 14, 2004. Claims 1-22 will be pending upon entry of the present amendment. Claim 10 is being amended.

Rejections Under 35 U.S.C. §102

Claims 1-5, 8-19 are rejected under 35 U.S.C. §102(e) as being anticipated by Ayers et al. (U.S. Patent 6,263,461).

Ayers is generally directed towards a testing circuitry for a memory array. The circuitry comprises a memory block 120, address multiplexer 304, address formatter 303, data multiplexor 302, and data formatter 301 (Figure 3).

Ayers does not disclose the features of claim 1. Claim 1 recites, *intra alia*, "a data generator for generating a predetermined bit pattern for writing to the memory." Ayers fails to disclose such a data generator that generates a predetermined bit pattern. First, the Ayers device does not generate a predetermined bit pattern for writing to the memory. The output of the data formatter 301 is based on the value of the input from the external "built in test controller" (*see e.g.*, Ayers, col. 5, lines 52-56). Ayers does not mention the predetermining of the input from the external controller. As the formatted output to the memory block is reliant on an external non-predetermined data source, the output to the memory block is not a predetermined bit pattern.

Further, the data formatter 301 as disclosed by Ayers is not a data generator, and should be more properly termed a data formatter. Ayers calls data formatter 301 a data generator, and asserts that the "BIST Data Generator 301 generates test data (Test Din)" (Ayers, col. 5, lines 52-53). However, the formatter clearly does not generate a bit pattern. Rather, the data formatter 301, has an formatted output (Test Din) and an unnamed input (*see e.g.*, Ayers, col. 5, lines 53-54). The unnamed input of the data formatter receives data from an external controller (*see e.g.*, Ayers, col. 5, lines 53-54). The data formatter 301 formats the input to produce the Test Din output (*see e.g.*, Ayers, col. 5, lines 54-55). The output is then coupled to the memory block 120 (*see e.g.*, Ayers, col. 5, line 55). As an external controller generates the

test data for formatting by data formatter, the Ayers device does not have internal means to generate test data patterns.

For the reasons discussed above, Ayers does not recite the features of claim 1. Accordingly, claim 1 is allowable.

Ayers does not disclose the features of claim 10. Claim 10 has been amended to recite, *intra alia*, "a data generator selectively coupled to the memory array for generating a predetermined bit pattern for writing to the memory ... ." As discussed above, Ayers neither discloses an output comprising a predetermined bit pattern, nor a data generator. Accordingly, claim 10 is not anticipated by Ayers, and is thus allowable.

Rejections Under 35 U.S.C. §103

Claims 6-7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ayers et al. (U.S. Patent 6,263,461) in view of Rapoport (U.S. Patent 5,557,619).

Ayers and/or Rapoport do not disclose, teach, or suggest the features recited by claims 6-7. Claims 6-7 depend on claim 1. As discussed above, Ayers fails to disclose a data generator for generating a predetermined bit pattern, as recited by claim 1. Further, Rapoport fails to disclose such a data generator. Finally, Ayers and/or Rapoport, even if combined, fail to teach or suggest any such a data generator. As the underlying basis for the rejection is not disclosed, taught, or suggested by Ayers and/or Rapoport, there can be no motivation for extension of the base claim, as recited by claims 6-7. Accordingly, any combination of the teachings of Ayers and Rapoport would not result in the features as recited by claims 6-7. Claims 6-7 are thus allowable.

New Claims

New claims 20- 22 are added. Claim 20 recites, *intra alia*, "coupling an output of the internal address counter with an input of the internal data generator; generating a predetermined bit pattern with the internal data generator based upon the value of the internal address counter ... ." As discussed above, neither Ayres and/or Rapoport, even in combination, disclose, teach or suggest the coupling of the address counter with the data generator, or the

generation of the predetermined bit pattern based on the address at which the data will be written. Accordingly, any combination of the teachings of Ayres and Rapoport would not result in the features as recited by claim 20. Claim 20 is thus allowable.

Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable.

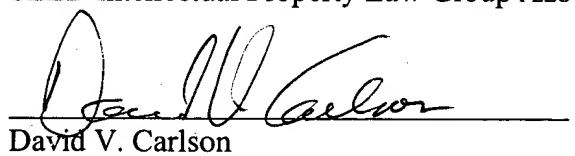
If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



David V. Carlson
Registration No. 31,153

DVC:lcs
Enclosure:
Postcard

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900 / Fax: (206) 682-6031

456633_1.DOC